



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,073	01/20/2004	Simon C. Steely JR.	200313630-1	3181
22879 7590 10/01/2009 HEWLETT-PACKARD COMPANY Intellectual Property Administration 3404 E. Harmony Road Mail Stop 35 FORT COLLINS, CO 80528				
EXAMINER				
CAMPOS, YAIMA				
ART UNIT		PAPER NUMBER		
2185				
NOTIFICATION DATE		DELIVERY MODE		
10/01/2009		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

JERRY.SHORMA@HP.COM
ipa.mail@hp.com
jessica.l.fusek@hp.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SIMON C. STEELY JR., GREGORY EDWARD TIERNEY, and
STEPHEN R. VAN DOREN

Appeal 2009-002631
Application 10/761,073¹
Technology Center 2100

Decided: September 29, 2009

Before LANCE LEONARD BARRY, JEAN R. HOMERE, JAY P.
LUCAS, *Administrative Patent Judges.*

LUCAS, *Administrative Patent Judge.*

DECISION ON APPEAL

¹ Application filed January 20, 2004. The real party in interest is Hewlett-Packard Development Co., LP.

STATEMENT OF THE CASE

Appellants appeal from a final rejection of claims 1 to 40 under authority of 35 U.S.C. § 134(a). The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

Appellants' invention relates to a method and system for maintaining cache coherency (providing accurate and consistent data) in a computer system in which the processors employ cache memory. In the words of Appellants:

[0024] This disclosure relates generally to systems and methods for conflict responses in a cache coherency protocol that supports migratory data. Migratory Data can be defined as a class of memory blocks that are shared by a plurality of processors and are characterized by a per processor reference pattern which includes a read and a write in close temporal proximity in the instruction stream of the processor. In general, such data blocks are expected to be shared in a manner in which each processor is provided with an opportunity to complete its read-write sequence before any other processors initiate their read-write sequence.

[0025] The per processor read-write sequence associated with Migratory Data can manifest itself in the system as a two-step per processor sequence consisting of a simple data read request (XREAD) followed by an upgrade (XUPGRADE) reference to make the line writable. An optimization is to reduce this two-step per processor sequence to a single step by implementing a single "Read with Modify Intent" (XRDWAL) request. Implementation of the single XRDINVAL request greatly reduces the latency of the request and reduces system request traffic. The cache coherency protocol described herein provides this optimized migratory data support through implementation of the XRDINVAL request.

[0026] Migratory data support is a system function implemented through the cache coherency protocol described herein. When a processor begins a migratory data sequence,

it encounters a read reference in its instruction stream that provides no indication that the read reference is operative on a migratory data line. Thus, when the read request is issued to the system by the processor, it is issued as a simple read request (XREAD). The cache coherency protocol described herein employs a predictive function to determine whether the read request is addressing a migratory data line. This predictive function can be a cache state decoding mechanism responsive to the states of all processors that are targets of snoops associated with the XREAD request. The predictive function implemented in the cache coherency protocol described herein covers a comprehensive set of coherence timing and conflict cases that can arise in during migratory data flows. Once migratory data is detected, the XREAD request is completed implementing measures to ensure that the XREAD is completed correctly.

[0027] The cache coherency protocol described herein supports migratory read commands by employing cache states (described in detail below) that function to predict whether a read command, or read snoop, involves migratory data. If a read snoop finds the requested line cached in a modified state in another cache, the data is returned to the requestor in a dirty state. Thus, in effect, when migration takes place, the migratory read command acts like a write command, moving the cache ordering point to the requesting node.

(Spec. 4, ¶24 to 5, ¶27).

Claims 1 and Claim 34 are exemplary:

Claim 1 A system comprising:

a first node that provides a source broadcast request for data, the first node being operable to respond in a first manner to other source broadcast requests for the data while the source broadcast request for the data is pending at the first node;

the first node being operable to respond in a second manner to the other source broadcast requests for the data in response to receiving an ownership data response at the first node, the ownership data response comprising a copy of the data.

Claim 34 A method comprising:

migrating a line of data and a cache ordering point for the line of data from a first node of a system to a second node of the system; and

issuing an invalidate line command for the line of data from the second node to other nodes of the system in response to receiving a conflict response from at least one other node in the system and to the cache ordering point migrating from the first node to the second node.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Arimilli	US 6,138,218	Oct. 24, 2000
(hereinafter "Arimilli 2")		(filed on Feb. 17, 1998)
Arimilli	US 2002/0129211 A1	Sep. 12, 2002
		(filed on Dec. 30, 2000)
Martin	US 6,883, 070 B2	Apr. 19, 2005
		(filed on Oct. 19, 2001)

REJECTIONS

The Examiner rejects the claims as follows:

- R1: Claims 1-9, 12-14, 16-22, 25-29, 31-37 and 39-40 stand rejected under 35 U.S.C. § 102(e) for being anticipated by Arimilli.
- R2: Claims 10-11, 23-24, 30 and 38 stand rejected under 35 U.S.C. § 103(a) for being obvious over Arimilli in view of Arimilli 2.
- R3: Claims 15 stands rejected under 35 U.S.C. § 103(a) for being obvious over Arimilli in view of Arimilli 2 and further in view of Martin.

Groups of Claims:

The claims will be discussed in the order of the rejections.

Appellants contend that the claimed subject matter is not anticipated by Arimilli or rendered obvious by Arimilli in combination with Arimilli 2 or Wang for failure of the references to teach claimed limitations and under 35 U.S.C. § 103(a) to be properly combined. The Examiner contends that each of the claims is properly rejected.

Rather than repeat the arguments of Appellants or the Examiner, we refer to the Briefs and the Answer for their respective details. Only those arguments actually made by Appellants have been considered in this opinion. Arguments that Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived.

We affirm the rejections.

ISSUE

The principal issue before us is whether Appellants have shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a). The issue turns on whether Arimilli alone or in conjunction with the other references teaches a first computing node operable to respond to source broadcast requests from other nodes for its data in two manners depending on whether that first node's own source broadcast is pending and other limitations as claimed.

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. Appellants have invented a system and method to help assure cache coherency of a multi-node computer system using rules of a coherency protocol (Spec. 7, ¶ [0036]). The protocol may be a hybrid cash coherency protocol, which switches from a broadcast source snoop protocol to a forward progress protocol if the snoop request fails because of a potential conflict (Spec. 7, ¶ [0037]). In either protocol, the type of response to a memory request depends on the state of the identified requested memory block, for example whether it is shared, owned, or in transition ((Spec. 8, ¶¶ [0039], [0040]; 9, Table 1). The sending of the data migrates the ordering point, the place of the “up-to-data” data, from the cache of the target processor to the cache of the source of the data request (Spec. 10, ¶ [0042]) To help avoid conflicts of data, while the requested data is being sent during migration of the ordering point, the cache line of the target (sending) node stays in a “transition” state (Spec. 10, ¶ [0043]). When the source processors safely receive the data, and the ordering point has thus successfully migrated, acknowledgements will clear the state of the cache line from the transition state to another state (*id.*).
2. Arimilli teaches a system and method for maintaining coherency in a multi-node computer system (¶ [0012]). In response to snooping a transaction, second or more agents (computers) respond indicating whether there will be a coherency conflict with the pending store request (*id.*). A coherency decision awaits a combined response from all the other

agents in the system. Following receipt of the combined response, the first agent assumes responsibility for the data (§ [0013]).

3. Arimilli 2 teaches a forward progress technique to obtain the required data while preserving the coherency of the system (Col. 6, l. 55 to 65).

PRINCIPLES OF LAW

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of prima facie obviousness or by rebutting the prima facie case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

"In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992).

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375 (Fed. Cir. 2005) (citation omitted).

It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. *See In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986) and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984).

“What matters is the objective reach of the claim. If the claim extends to what is obvious, it is invalid under § 103.” *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398 at 419 (2007). To be nonobvious, an improvement must be “more than the predictable use of prior art elements according to their established functions.” *Id.* at 401.

Our guiding court has held “The prior art’s mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claims in the ’198 application.” (*In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004)).

ANALYSIS

From our review of the administrative record, we find that the Examiner has presented a prima facie case for the rejections of Appellants’ claims under 35 U.S.C. §§ 102 and 103 on pages 3 to 28 of the Examiner’s Answer. In opposition, Appellants present a number of arguments.

*Arguments with respect to the rejection
of claims 1 to 9, 12 to 14, 16 to 22, 25 to 29, 31 to 37 and 39 to 40
under 35 U.S.C. § 102(b) [R1]*

Appellants contend that “Arimilli fails to disclose a first node that provides a source broadcast request for data.” (App. Br. 22, middle). In the Arimilli reference, the various nodes are called agents ([¶¶ 0021], [0022]). The Examiner presents a number of places in Arimilli where agents present broadcasts requests for data, serving as the source agent (Ans. 29, middle). Considering just one of those references, paragraph [0029], we note processor complex 10a issuing a command that requires a request for data,

intending to modify it after gaining ownership to it. Similar references are found in paragraphs [0026], [0025], and [0035] to [0038]. In each reference we note an explicit or an inherent request for data. We decline to find error in the rejection on this point.

Appellants next contend that Arimilli fails to “disclose the first and second manner of responding, as recited in claim 1.” (App. Br. 25, middle). We note with agreement the Examiner’s comment in the Answer, page 31, observing that the claims do not require that the first and second manners of responding be different. Nonetheless, as discussed in the reference, paragraph [0032], the coherency decision points (CDPs) arbitrate the relative rights to control the data, to produce a combined response to a request for data. Until this combined response is accomplished, the CDP protects the grant of ownership with appropriate snoop responses (§ [0013]). This is read on the claimed first manner of responding while the request is pending. After the receipt of the combined response, the first agent assumes responsibility for the protection of the data, other agents acquiesce to invalidation of their cached copies of the data, and agents do not modify their local copies (*id.*). That is a claimed first node being operable to respond in a second manner. There is also a teaching in paragraph [0031] of the CDP granting ownership to the source agent 10, engendering the manner of response associated with its snooper being the next CDP. We thus do not find error in the Examiner’s rejection being shown by this argument.

Appellants next argue that Arimilli does not disclose “a first node . . . receiving an ownership data response comprising a copy of the data.” (Brief 27, middle). We have reviewed the Examiner’s Answer and agree that Arimilli clearly teaches a broadcast request answered by being “provided an

up-to-date copy of a target cache line” at (¶ [0006]) and at other locations noted in the reference (Ans. 32-33).

We thus do not find error in the rejection [R1] of claim 1.

We have considered Appellants’ other arguments concerning independent claims 16, 25, 31, 34, 39 and 40 and the claims dependent on those claims rejected under 35 U.S.C. § 102(b) [R1]. In each case the Examiner’s arguments are not shown to be of error.

*Arguments with respect to the rejection
of claims 10 to 11, 23 to 24, 30 and 38
under 35 U.S.C. § 103(a) [R2]*

The Examiner has rejected the cited claims for being obvious over Arimilli in view of Arimilli 2. Appellants first contend that the reference “Arimilli 2 fails to make up for the deficiencies of Arimilli.” (App. Br. 57, bottom). As we found no such deficiencies, this argument is considered negated.

Appellants next contend that as Arimilli does not teach using a forward progress technique but teaches another method of ownership, it cannot be combined with any other teaching as it teaches away from the claims (App. Br. 58, bottom). However, since we do not find in Arimilli any explicit statement that will “criticize, discredit, or otherwise discourage” a forward progress technique, we will follow the standard of *In re Fulton*, 391 F.3d at 1201, and disagree that the reference is “teaching away” from the disclosure of a forward progress technique being combined with Arimilli.

Concerning Appellants’ other arguments addressing the rejections of the dependent claims of this rejection [R2], we adopt and endorse the

Examiner's reasoning on pages 51 through 54 of the Answer, and decline to find error in this rejection.

*Arguments with respect to the rejection
of claim 15
under 35 U.S.C. § 103(a) [R3]*

The Examiner has rejected claim 15 for being obvious over Arimilli, Arimilli 2, and Martin. Appellants' first argument addresses teachings of forward progress coherency cache protocol in Arimilli 2, which the Examiner has sufficiently addressed in her response to rejection [R2] (App. Br. 60, bottom) (See above discussion.) We do not find error.

Concerning Appellants' remaining arguments about switching protocols and motivation to combine, we adopt and endorse the Examiner's remarks (Ans. 56). We thus do not find error in the rejection of claim 15. (R3).

CONCLUSIONS OF LAW

Based on the findings of facts and analysis above, we conclude that the Examiner did not err in rejecting claims 1-40 respectively under rejections [R1], [R2] and [R3].

DECISION

The Examiner's rejections [R1], [R2], and [R3] of claims 1-40 are affirmed

AFFIRMED

Appeal 2009-002631
Application 10/761,073
peb

HEWLETT-PACKARD COMPANY
INTELLECTUAL PROPERTY ADMINISTRATION
3404 E. HARMONY ROAD
MAIL STOP 35
FORT COLLINS CO 80528